ETS-EVO

Follows a collection of information related to the ETS-EVO board in order to be able to customize its functional behaviour.

SERIAL PORTS

ttyUL0: GNU/Linux serial console over DB9 (115200/8-N-1)
ttyUL1: GPS module (9600/8-N-1)
ttyUL2: custom serial stream over DB9 (custom conf)

please note that ttyUL0 and ttyUL2 share the same DB9 connector on the back and may be activated via a switch in the COUNTER_CTRL register.

ETHERNET PORTS

eth0: 10/100 Mbps (PTPv2, SyncE)
eth1: 10/100 Mbps (PTPv2, SyncE)

FLASH

0x88000000: 16 MB (Numonyx J3D)

RAM

0x90000000: 128 MB (Micron DDR3)

PWM OCXO

0x83C10000: timer1

INTERRUPTS

10: PPS

REGISTER MAP

HW_RELEASE 0x81400000
Read-only
[31..0] hardware version

COUNTER_VALUE 0x81400004
Read-only
[31..0] trigger of the GPS pulse

PPS_VALUE 0x81400008
Read-only
[31..0] trigger of the internal PPS pulse

COUNTER_SEC 0x8140000C
Read-only
[31..0] unused. Read as 0

COUNTER_VALUE_IRIGB 0x81400010
Read-only
[31..0] trigger of the IRIG-B pulse

COUNTER_NSEC_PPS 0x81400014
Read-only
[31..0] elapsed ticks from the start of the internal PPS pulse

COUNTER_NSEC_GPS 0x81400018
Read-only
[31..0] elapsed ticks from the start of the GPS pulse

COUNTER_NSEC_IRIGB 0x8140001C
Read-only
[31..0] elapsed ticks from the start of the IRIG-B pulse

COUNTER_VALUE_ETH 0x81400020
Read-only
[31..0] elapsed ticks from the start of the ETH0 pulse

COUNTER_VALUE_ETH2 0x81400024
Read-only
[31..0] elapsed ticks from the start of the ETH1 pulse

IRIGB_RX_VECT_LO 0x81400028
Read-only
Contains the lower part of the incoming IRIG-B stream
[6..0] seconds in BCD format
[13..7] minutes in BCD format
[19..14] hours in BCD format
[31..20] day of year in BCD format

IRIGB_RX_VECT_HI 0x8140002C
Read-only
Contains the upper part of the incoming IRIG-B stream
[7..0] year in BCD format

IRIGB_TX_VECT_LO 0x81400030
Read-write
Contains the lower part of the outgoing IRIG-B stream
[6..0] seconds in BCD format
[13..7] minutes in BCD format
[19..14] hours in BCD format
[31..20] day of year in BCD format

IRIGB_TX_VECT_HI 0x81400034
Read-write
Contains the upper part of the outgoing IRIG-B stream
[7..0] year in BCD format

COUNTER_CTRL 0x81400038
Read-write
[0] reserved
[1] resync PPS on GPS
[2] ticks read for GPS
[3] ticks read for IRIG-B
[4] resync on ETH1
[5] resync on ETH0
[6] resync on IRIG-B
[9..7] PPS0 multiplexer
    0: PPS
    1: IRIG-B
    2: PULSE #1
    3: PULSE #2
    4: CLOCK #1
    5: CLOCK #2
[12..10] PPS1 multiplexer (as for PPS0)
[13] IRIG-B input multiplexer
    0: BNC
    1: OPTICAL
[14] just resync PPS, but leave other processes untouched (e.g. IRIG-B generation)
[15]: ticks read for internal PPS
[17..16] UART multiplexer
    0: no output
    1: custom uart
    2: serial console
[19..18] disciplining multiplexer
    0: pwm from timer1
    1: syncE from eth0
    2: syncE from eth1
[21..20] syncE hold for eth0
    0: disciplining active
    1: holdover
[23..22] syncE hold for eth1 (as for eth0)
[24] reboot
[27..25] IRIG-B output multiplexer (as for PPS0)
[31..28] output leds

COUNTER_CTRL2 0x8140003C
Read-write
[6..0] electrical status of the external relays outputs

OPTO1BLOCK 0x81400040
Read-only
[5..0] electrical status of the external opto-coupled inputs

IRIGB_TX_SDAY 0x81400044
Read-write
[31..0] seconds in the day. Updated by software to trigger time-driven events in hardware

IRIGB_PULSE_START 0x81400048
Read-write
[31..0] seconds in the day to start the pulse (shared between pulse0 and pulse1)

IRIGB_PULSE_STOP 0x8140004C
Read-write
[31..0] seconds in the day to stop the pulse (shared between pulse0 and pulse1)

IRIGB_PULSE_RATE 0x81400050
Read-write
[31..0] repetition rate of the pulse in seconds (shared between pulse0 and pulse1)

IRIGB_PULSE_LEN 0x81400054
Read-write
[31..0] Length of the pulse in 0.1 milliseconds (shared between pulse0 and pulse1)

IRIGB_PULSE_EN 0x81400058
Read-write
[0] pulse0 enable
[1] pulse1 enable
[15] pulse0 active
[16] pulse1 active

IRIGB_PULSE_MUX 0x8140005C
Read-write
[31..0] pulse number

CLOCK1_DIV 0x81400060
Read-write
[31..0] clock divider for the 10 MHz

CLOCK2_DIV 0x81400064
Read-write
[31..0] clock divider for the 16.384 MHz

TCSR0 0x83C10000
Read-write
[31..0] Timer control register 1 (0x216 for PWM operation)

TLR0 0x83C10004
Read-write
[31..0] Period value

TCSR1 0x83C10010
Read-write
[31..0] Timer control register 2 (0x616 for PWM operation)

VTUNE_VALUE 0x83C10014
Read-write
[31..0] duty cycle